

CLAIM AMENDMENTS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently Amended) A data processing system, comprising:
 - 2 | a first integrated circuit, the first integrated circuit ~~including comprising~~:
 - 3 | a first logic block ~~eonfigured to generate~~ generating a data stream;
 - 4 | a hardware encryption circuit coupled to the first logic block, and ~~configured to encrypt~~ the hardware encryption circuit encrypting the data
 - 5 | stream to generate an encrypted data stream; and
 - 6 |
 - 7 | a first Peripheral Component Interconnect Express (PCI-Express) -
8 | compatible interface circuit ~~eonfigured to support~~ supporting data
9 | communication over a plurality of PCI-Express virtual channels, wherein the
10 | plurality of PCI-Express virtual channels ~~includes~~ comprises at least an
11 | unencrypted default virtual channel and a dedicated encrypted virtual
12 | channel, ~~that is incapable of being bypassed or disabled, and is configured to~~
13 | ~~communicate encrypted data exclusively,~~ wherein the first PCI-Express-
14 | compatible interface circuit includes a first plurality of channel interconnects,
15 | each channel interconnect associated with a virtual channel among the
16 | plurality of virtual channels, wherein a first channel interconnect among the
17 | plurality of virtual channels is coupled to the hardware encryption circuit to

18 receive the encrypted data stream, and wherein the first PCI-Express-
19 compatible interface circuit ~~is configured to communicate~~ communicates the
20 encrypted data stream from the hardware encryption circuit over the
21 dedicated encrypted virtual channel;
22 a second integrated circuit coupled to the first integrated circuit by a PCI-
23 Express-compatible interconnect, the second integrated circuit—including
24 comprising:
25 a second PCI-Express-compatible interface circuit coupled to the PCI-
26 Express-compatible interconnect to receive the encrypted data stream over
27 the dedicated encrypted virtual channel, the second PCI-Express-compatible
28 interface circuit ~~including comprising:~~
29 a second plurality of channel interconnects, each channel
30 interconnect associated with a virtual channel among the plurality of
31 virtual channels;
32 a hardware decryption circuit coupled to a first channel
33 interconnect among the second plurality of channel interconnects for
34 the second PCI-Express-compatible interface circuit and configured to
35 decrypt the encrypted data stream; and
36 a second logic block coupled to the hardware decryption circuit
37 and configured to use the decrypted data stream; and

38 control logic coupled to at least one of the first and second PCI-Express-
39 compatible interface circuits and configured to communicate authorization data
40 over the default virtual channel to authorize secure communication between the
41 first and second integrated circuits over the dedicated encrypted virtual channel,
42 wherein all data sent over the dedicated encrypted virtual channel are encrypted,
43 and access control and decoding are separately performed on the first and second
44 integrated circuits for the dedicated encrypted virtual channel.

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1 2. (Currently Amended) A circuit arrangement, comprising:

2 a multi-channel serial interface circuit configured to communicate data over a
3 serial interconnect using a plurality of virtual channels; and
4 a hardware encryption circuit coupled to the multi-channel serial interface
5 circuit and configured to encrypt all data communicated over a dedicated encrypted
6 virtual channel, ~~that is incapable of being bypassed or disabled~~, among the plurality
7 of virtual channels,

8 wherein all data sent over the dedicated encrypted virtual channel are
9 encrypted, and access control and decoding are separately performed on two
10 integrated circuits for the dedicated encrypted virtual channel.

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1 3. (Previously Presented) The circuit arrangement of claim 2, the multi-channel
2 serial interface circuit further comprising:

3 PCI-Express-compatible interface logic coupled to the hardware encryption
4 circuit and configured to communicate encrypted data output by the hardware
5 encryption circuit over a PCI-Express-compatible interconnect.

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1 4. (Previously Presented) The circuit arrangement of claim 2, further
2 comprising:

3 a logic block coupled to the hardware encryption circuit and configured to
4 output data for communication over the serial interconnect to the hardware
5 encryption circuit such that the data output by the logic block is encrypted prior to
6 communication over the serial interconnect.

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1 5. (Original) The circuit arrangement of claim 4, wherein the logic block is
2 additionally configured to output additional data for communication over an
3 unencrypted virtual channel among the plurality of virtual channels.

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1 6. (Original) The circuit arrangement of claim 4, wherein the logic block is
2 configured to output data over the serial interconnect solely over the dedicated
3 encrypted virtual channel.

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1 7. (Previously Presented) The circuit arrangement of claim 4, further
2 comprising:

3 a second logic block coupled to the multi-channel serial interface circuit and
4 configured to output data for communication over an unencrypted virtual channel
5 among the plurality of virtual channels.

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1 8. (Previously Presented) The circuit arrangement of claim 4, further
2 comprising:

3 a second logic block coupled to the hardware encryption circuit and
4 configured to output data for communication over the dedicated encrypted virtual
5 channel.

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1 9. (Previously Presented) The circuit arrangement of claim 4, further
2 comprising:

3 a hardware decryption circuit coupled intermediate the multi-channel serial
4 interface circuit and the logic block, the hardware decryption circuit configured to
5 decrypt encrypted data received from the serial interconnect by the multi-channel
6 serial interface circuit and communicated over the dedicated encrypted virtual
7 channel.

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1 10. (Original) The circuit arrangement of claim 4, wherein the plurality of virtual
2 channels includes a default virtual channel configured to communicate

3 authorization data for authorizing secure communication over the dedicated
4 encrypted virtual channel.

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1 11. (Previously Presented) An integrated circuit comprising:
2 the multi-channel serial interface circuit and hardware encryption circuit of
3 claim 2.

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1 12. (Previously Presented) A data processing system, comprising:
2 the integrated circuit of claim 11, and
3 a second integrated circuit comprising:
4 a second multi-channel serial interface circuit configured to receive the
5 encrypted data communicated over the serial interconnect by the first multi-
6 channel serial interface circuit, and
7 a hardware decryption circuit configured to decrypt the encrypted data
8 received over the serial interconnect.

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1 13. (Canceled)

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1 14. (Currently Amended) A circuit arrangement, comprising:
2 a multi-channel serial interface circuit configured to communicate data over a
3 serial interconnect using a plurality of virtual channels; and

4 a hardware decryption circuit coupled to the multi-channel serial interface
5 circuit and configured to decrypt all data received from the serial interconnect by
6 the multi-channel serial interface that has been communicated over the serial
7 interconnect on a dedicated encrypted virtual channel, ~~that is incapable of being~~
8 bypassed or disabled, among the plurality of virtual channels, wherein all data sent
9 over the dedicated encrypted virtual channel are encrypted and access control, and
10 decoding are performed on two separate integrated circuits for the dedicated
11 encrypted virtual channel.

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1 15. (Currently Amended) A method of communicating data over a serial
2 interconnect, the method comprising:

3 encrypting a data stream using a hardware encryption circuit disposed on ~~an~~
4 a first integrated circuit; and
5 communicating the encrypted data stream over a serial interconnect using a
6 multi-channel serial interface circuit disposed on the first integrated circuit,
7 wherein communicating the encrypted data stream includes communicating the
8 encrypted data stream over a dedicated encrypted virtual channel, ~~that is incapable~~
9 ~~of being bypassed or disabled,~~ from among a plurality of virtual channels supported
10 by the multi-channel serial interface circuit, ~~and~~ wherein the dedicated encrypted
11 virtual channel is dedicated to the communication of encrypted data, and wherein
12 all data sent over the dedicated encrypted virtual channel are encrypted, and access

13 control and decoding are separately performed on two integrated circuits for the
14 dedicated encrypted virtual channel.

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16. (Currently Amended) The method of claim 15, further comprising:
2 communicating the encrypted data over a PCI-Express-compatible
3 interconnect, wherein the multi-channel serial interface circuit comprises PCI-
4 Express-compatible interface logic coupled to the hardware encryption circuit, and
5 wherein communicating the encrypted data stream over the serial interconnect
6 comprises communicating the encrypted data over a PCI Express compatible
7 interconnect.

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17. (Previously Presented) The method of claim 15, further comprising:
2 generating the data stream from a logic block disposed on the integrated
3 circuit.

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18. (Currently Amended) The method of claim 17, further comprising:
2 configuring wherein the logic block is configured to output data over the
3 serial interconnect solely over the encrypted virtual channel.

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19. (Previously Presented) The method of claim 17, further comprising:

2 generating a second data stream from a second logic block disposed on the
3 integrated circuit, and

4 communicating the second data stream over the serial interconnect using an
5 unencrypted virtual channel among the plurality of virtual channels supported by
6 the multi-channel serial interface circuit.

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1 20. (Original) The method of claim 17, further comprising:
2 decrypting a second encrypted data stream received from the serial
3 interconnect by the multi-channel serial interface circuit and communicated over
4 the dedicated encrypted virtual channel using a hardware decryption circuit
5 disposed on the integrated circuit; and
6 communicating the decrypted data stream to the logic block.

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1 21. (Previously Presented) The method of claim 17, wherein the plurality of
2 virtual channels includes a default virtual channel, the method further comprising:
3 communicating authorization data over the default virtual channel to
4 authorize secure communication over the dedicated encrypted virtual channel.

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1 22. (Original) The method of claim 17, further comprising:

2 receiving the encrypted data stream from the serial interconnect using a
3 second multi-channel serial interface circuit disposed on a second integrated circuit;
4 and

5 decrypting the encrypted data stream using a hardware decryption circuit
6 disposed on the second integrated circuit.

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2 23. (Currently Amended) A method of providing access control for a digital data
stream, the method comprising:

3 decrypting a first encrypted data stream in a first integrated circuit to
4 generate a first decrypted data stream;

5 re-encrypting the first decrypted data stream in the first integrated circuit to
6 generate a second encrypted data stream;

7 communicating the second encrypted data stream from the first integrated
8 circuit to a second integrated circuit over a multi-channel serial interconnect to
9 which the first and second integrated circuits are connected by communicating the
10 second encrypted data stream over a dedicated encrypted virtual channel, ~~that is~~
11 ~~ineapable of being bypassed or disabled, among a plurality of virtual channels~~
12 ~~supported by the multi-channel serial interconnect, wherein all data sent over the~~
13 ~~dedicated encrypted virtual channel are encrypted and access control, and decoding~~
14 ~~are performed separately on the first and second integrated circuits for the~~
15 ~~dedicated encrypted virtual channel; and~~

16 decrypting the second encrypted data stream in the second integrated circuit
17 to generate a second decrypted data stream.

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2 24. (Previously Presented) The method of claim 23, further comprising:
3 demodulating a modulated input signal to generate the first encrypted data
4 stream.

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2 25. (Previously Presented) The method of claim 24, further comprising:
3 decoding the second decrypted data stream in the second integrated circuit to
4 generate a decoded data stream.

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2 26. (Currently Amended) The method of claim 24, further comprising:
3 performing MPEG decoding on the second decrypted data stream, wherein
4 the modulated input signal comprises a satellite broadcast signal, and wherein the
5 first encrypted data stream comprises an encrypted MPEG data stream, and
6 wherein decoding the second decrypted data stream in the second integrated circuit
7 comprises performing MPEG decoding on the second decrypted data stream.

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2 27. (Currently Amended) The method of claim 23, further comprising:
3 wherein decrypting the first encrypted data stream includes
4 performing regional access control on the first encrypted data stream.

1 28. (Currently Amended) The method of claim 23, further comprising:
2 ~~wherein decrypting the first encrypted data stream includes~~
3 performing subscriber access control on the first encrypted data stream.

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2 29. (Currently Amended) The method of claim 23, further comprising:
3 ~~wherein~~
4 ~~disposing~~ the first and second integrated circuits are disposed in a set top
box.

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2 30. (Currently Amended) The method of claim 23, further comprising:
3 ~~wherein~~
4 ~~disposing~~ the first integrated circuit is disposed on an access card coupled to
the second integrated circuit via a connector.

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2 31. (Currently Amended) The method of claim 23, further comprising:
3 ~~wherein~~
4 ~~performing re-encrypting re-encryption of the first decrypted data stream is~~
5 ~~performed by~~ with hardware encryption logic disposed on the first integrated
circuit.

- 1 32. (Currently Amended) A circuit arrangement, comprising:
- 2 first decryption logic configured to perform access control and to decrypt a
3 first encrypted data stream and generate therefrom a first decrypted data stream,
4 the first decryption logic disposed on a first integrated circuit in a processor chip
5 set;
- 6 encryption logic configured to re-encrypt the first decrypted data stream and
7 generate therefrom a second encrypted data stream;
- 8 decoder logic on a second integrated circuit in the processor chip set; and
- 9 a multi-channel serial interface circuit configured to communicate the second
10 encrypted data stream over a multi-channel serial interconnect by communicating
- 11 the second encrypted data stream over a dedicated encrypted virtual channel, that
12 is incapable of being bypassed or disabled, among a plurality of virtual channels
13 supported by the multi-channel serial interconnect, wherein all data sent over the
14 dedicated encrypted virtual channel are encrypted and access control, and decoding
15 are performed separately on the first and second integrated circuits for the
16 dedicated encrypted virtual channel.
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- 1 33. (Currently Amended) The circuit arrangement of claim 32, further
2 comprising:
- 3 second decryption logic configured to decrypt decrypting the second encrypted
4 data stream and generating generate therefrom a second decrypted data stream.

1 34. (Currently Amended) The circuit arrangement of claim 33, further
2 comprising:

3 | demodulation logic ~~configured to generate~~~~generating~~ the first encrypted data
4 | stream from a modulated input signal.

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2 | 35. (Currently Amended) The circuit arrangement of claim 34, further
3 | ~~comprising:wherein the decoder logic configured to decode~~~~decodes~~ the second
3 | decrypted data stream.

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2 | 36. (Original) The circuit arrangement of claim 35, wherein the modulated input
3 | signal comprises a satellite broadcast signal, wherein the first encrypted data
4 | stream comprises an encrypted MPEG data stream, and wherein decoding the
5 | second decrypted data stream in the second integrated circuit comprises performing
5 | MPEG decoding on the second decrypted data stream.

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2 | 37. (Currently Amended) The circuit arrangement of claim 35, wherein the
3 | demodulation logic, ~~the first decryption logic~~, the encryption logic, and the multi-
4 | channel serial interface circuit are disposed on a ~~the~~ first integrated circuit,
5 | wherein the second decryption logic and ~~decoder logic~~ are ~~is~~ disposed on a ~~the~~
5 | second integrated circuit, and wherein the second integrated circuit includes a

6 second multi-channel serial interface circuit coupled to the multi-channel serial
7 | interconnect to receive the second encrypted data stream ~~therefrom~~.

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2 38. (Currently Amended) The circuit arrangement of claim 32, wherein the first
decryption logic ~~is configured to perform~~ performs regional access control on the
3 first encrypted data stream.

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2 39. (Currently Amended) The circuit arrangement of claim 32, wherein the first
decryption logic ~~is configured to perform~~ performs subscriber access control on the
3 first encrypted data stream.

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2 40. (Currently Amended) The circuit arrangement of claim 32, wherein the
multi-channel serial interface circuit comprises PCI-Express-compatible interface
3 | logic coupled to the encryption logic, ~~and configured to communicate~~ communicating
4 the first encrypted data stream over a PCI-Express-compatible interconnect.

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2 41-45. (Canceled)